3rd IEEE International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA-2022)

DAY 1

Tutorial and Workshop Sessions – December 16, 2022 (Friday)

Tutorial and Workshop Venue: Krishna Hall (Pre-Lunch) and VLSI Lab (Post Lunch)	
09.00 AM to 10.00 AM	Registration
10.00 AM to 11.30 AM	Tutorial "VLSI Fab and Demystified" Dr. N. S. Murthy, Consultant to LeCo Consulting, Bengaluru
11.30 AM to 11.45 AM	*Tea/Coffee Break*
11.45 AM to 13.30 PM	Tutorial Session Contd…
13.30 PM to 14.00 PM	*Networking over Lunch*
14.00 PM to 15.30 PM	Workshop "System Design Flow Using Xilinx Vivado and Vitis on PYNQ Z2 Board" Mr. Sharan A, CoreEL Technologies, Bengaluru
15.30 PM to 15.45 PM	*Tea/Coffee Break*
15.45 PM to 17.00 PM	Workshop Session Contd…
End of the first day	

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DAY 2

Conference - December 17, 2022 (Saturday)

Plenary Session (Venue: Krishna Hall)	
08.15 AM to 09.00 AM	Registration
09.00 AM to 09.05 AM	Lighting the Lamp and Invocation Song
09.05 AM to 09.10 AM	Welcome Address
09.10 AM to 09.13 AM	Conference Chair Address
09.13 AM to 09.15 AM	IEEE VTS Founder Chair Address
09.15 AM to 09.25 AM	Dr. Sriram Devanathan Principal, ASEB
09.25 AM to 09.30 AM	Dr. Manoj P., Director, ASEB
09.30 AM to 09.50 AM	Chief Guest Address Mr. Hemant Mallapur Co-founder & Exec. VP Engineering, Saankhya Labs
09.50 AM to 09.55 AM	Technical Program Committee Chair Address
09.55 AM to 10.40 AM	Inauguration Keynote Address Dr. Parthasarathy Ramaswamy, Senior Principal Engineer at Intel Corporation
10.40 AM to 10.45 AM	*Photo session*
10.45 AM to 11.15 AM	*Tea/Coffee Break*

11.15 AM to 12.00 PM	**Keynote Address 1** **Mr. Prasanna Thyamagondlu, Director – Product development, Capgemini**	
Technical Paper Presentation sessions **The duration of each paper presentation is 20 mins (15 mins for presentation and 5 mins for Q & A)**		
Technical Tracks:	**TRACK 1 - VLSI Technology** **Venue – Krishna Hall** **External Session Chair: Dr. Jalaja S.** **Internal Session Chair: Dr. Kamatchi S.**	**TRACK 2 - VLSI Technology** **Venue – Rama Hall** **Internal Session Chair : Dr. M. Vinodhini**
12.05 PM to 12.25 PM	**Paper ID: 23** Performance Analysis of Dielectric Engineered Negative Capacitance Tunnel FETs Midhun Das P., Shikha U. S., Rekha K James, Anju Pradeep and Harikumar K. R., Cochin University of Science and Technology, Kerala	**Paper ID: 42** Comparative Study of Junctionless and Inverted Mode FinFET for Detection of Breast Cancer Cell HS578t at Microwave Frequency Himani Sehgal, Yogesh Pratap and Sneha Kabra, Shaheed Rajguru College of Applied Sciences for Women, University of Delhi
12.25 PM to 12.45 PM	**Paper ID: 26** Gain Enhancement of Cage Shaped Antenna using Frequency Selective Surface for mm-wave Applications Arun T. R., Sajith K., Jobin Jose and Salija P., Govt. Engg. College, Wayanad.	**Paper ID: 52** Mathematical Modeling of Annealed Trilayer Oxide-based Memristor Device Paramasivam K., Nithya N. and A. Napolean Kumaraguru College of Technology, Tamil Nadu
12.45 PM to 13.05 PM	**Paper ID: 83** Effective Hubbard Parametrization for Optimizing Electronic Bandgap of Monolayer CrI3 Kandarpa Dinesh Krishna, Rahul Nair, T.U. Shilpa Sree, Shamik Chakraborty and Abhilash Ravikumar Amrita School of Engineering, Bengaluru	

13.05 PM to 14.00 PM	**Networking over Lunch**		
14.00 PM to 14.45 PM	**Keynote Address 2** **Mr. Vaibhav Pratap Singh** **Principal Technical Officer, CDAC Bangalore**		
Technical Tracks:	**TRACK 3 - VLSI Systems** **Venue – Krishna Hall** **External Session Chair** **Dr. Rashmi Seethur** **Internal Session Chair** **Dr. Chintala Ramesh**	**TRACK 4 - VLSI Applications** **Venue – Valmiki Hall** **External Session Chair** **Dr. Pushpa Mala S.** **Internal Session Chair** **Dr. Ganapathi Hegde**	**TRACK 5 - VLSI Architectures** **Venue – Rama Hall** **External Session Chair** **Ms. Roopa K Swamy** **Internal Session Chair** **Dr. Paramasivam**
14.50 PM to 15.10 PM	**Paper ID: 57** Programmable Pulse Shaping Amplifier for High Speed and High Resolution X-Ray Spectroscopy Prasanta Sarkar, Bharath M., and Shashikala V., U. R. Rao Satellite Centre, Bangalore	**Paper ID: 21** Noise Optimization and Linearization of RF Mixer using Inductive Peaking and Source Degeneration for Radio Local Area Network and Low Power Wireless Access System Applications Avvaru Subramanyam and R.V.S. Satyanarayana, Sri Venkateswara University College of Engineering, Tirupati	**Paper ID: 2** A Modular Scan Design Verification Approach for Multi-channel Mode Anurag Chandan, Deepali Koppad, and Vinayaka R Karanji, Ramaiah Institute of Technology, Bangalore
15.10 PM to 15.30 PM	**Paper ID: 24** Area Efficient VLSI design for Image Processing using the Modified CORDIC Algorithm Roshan Anil, Sampath Puppala and P. Sathish Kumar, Amrita School of Engineering, Bengaluru	**Paper ID: 25** CPW fed Metamaterial loaded Octagonal U-Shape Slotted Antenna for WBAN Applications Rithika, Arun T. R., Sajith K., Jobin Jose and Salija P., Govt. Engg. College, Wayanad.	**Paper ID: 18** An Enhanced Clock Tree Synthesis Methodology for Optimizing Power in Physical Design Anirudh .S. and T. K. Ramesh, Amrita School of Engineering, Bengaluru

15.30 PM to 15.50 PM	**Paper ID: 75** Influence of Coolant Inlet Temperatures on the Performance of Microchannel Heat Sink for Thermal Management of Heterogeneous Integrated Systems A. Ramakrishna, M. Muralidhara Rao and A. V. Sita Rama Raju Jawaharlal Nehru Technological University Kakinada	**Paper ID: 27** A Micro-Size CB-CPW Fed Implantable Antenna for High-Frequency ISM Band Applications Sweety T. J., Arun T. R., Sajith K., Jobin Jose and Salija P., Govt. Engg. College, Wayanad.	**Paper ID: 44** An Inaccurate Median Filter Architecture for Salt and Pepper Noise Removal Midde Venkata Siva and Jayakumar E. P., NIT, Calicut
15.50 PM to 16.10 PM	**Paper ID: 62** Investigation on Power Supply Scaling Effects on the Performance of PET/NET TSPC-DATA-Flip Flops at Wide Range of Operating Temperatures Nagavelly Tarun Teja, Kondapaka Karthikeya and J AJAYAN, SR University, Warangal	**Paper ID: 49** A New Constant Coefficient Multiplier for Deep Neural Network Accelerators Manoj B. R., Jayashree S Yaji and Raghuram S., M S Ramaiah Institute of Technology, Bangalore	**Paper ID: 37** Residue Adder Design for the Modulo Set {2^{n}-1, 2^{n},2^{n+1}} and its Application in DCT Architecture for HEVC P. Kopperundevi and M. Surya Prakash, NIT, Calicut
16.10 PM to 16.30 PM	**Paper ID: 66** A Proposal for Programmable Pattern Generator and its FPGA Implementation Geethu Remadevi Somanathan and Ramesh Bhakthavatchalu, Amrita School of Engineering, Amritapuri	**Paper ID: 3** Effects of Temperature Induced Phase Transition in Bulk CdS Structures Gatla Sumanth Reddy, Adiraju Lakshmi Sowmya, Akshara Pudhota, Shamik Chakraborty and Abhilash Ravikumar Amrita School of Engineering, Bengaluru	**Paper ID: 68** Design And Implementation of Mac by using Efficient Posit Multiplier T Keerthi and Yashu Swami, Aditya Engineering College, Andhra Pradesh
16.35 PM to 16.40 PM	**Distribution of Certificates**		
16.40 PM to 16.45 PM	**Announcement of Best Paper Award**		
16.40 PM to 16.50 PM	**Vote of Thanks**		